WHAT IS CLAIMED IS:

1. A memory merged with logic (MML) semiconductor device comprising:

a memory area having a self-aligned contact structure and a logic area having a dual gate structure including n-type metal oxide semiconductor (NMOS) and p-type metal oxide semiconductor (PMOS) being integrated together;

the memory area including:

a polycide gate electrode;

a hard mask pattern formed on the polycide gate electrode and comprised of nitride materials;

a spacer formed along the sidewall of the polycide gate electrode and comprised of nitride materials; and

a self-aligned contact formed between the adjacent spacers and being electrically connected with an impurity implantation region formed on a semiconductor substrate,

the logic area including:

salicided NMOS and PMOS gate electrodes; and

salicided source/drain regions; and

wherein a height of the polycide gate electrode is smaller than a height of the NMOS and PMOS gate electrodes.

2. The MML semiconductor device of claim 1, wherein the polycide gate electrode comprises a gate conductive pattern comprised of silicon and doped with conductive type impurities, and a silicide pattern.

3. The MML semiconductor device of claim 1, wherein the gate conductive pattern is a polysilicon pattern; and

the silicide pattern is a tungsten silicide pattern.

4. The MML semiconductor device of claim 1, wherein the NMOS gate electrode comprises a gate conductive pattern comprised of silicon and doped with n-type impurities; and

a silicide pattern formed by a self-aligned silicide (SALICIDE) process.

5. The MML semiconductor device of claim 4, wherein the gate conductive pattern is a polysilicon pattern; and

the silicide pattern is a cobalt silicide pattern.

6. The MML semiconductor device of claim 1, wherein the PMOS gate electrode comprises a gate conductive pattern comprised of silicon and doped with p-type impurities, and a silicide pattern formed by a SALICIDE process.

7. The MML semiconductor device of claim 6, wherein the gate conductive pattern is a polysilicon pattern; and

the silicide pattern is a cobalt silicide pattern.

8. The MML semiconductor device of claim 1, wherein the polycide gate electrode and the salicided NMOS and PMOS gate electrodes comprise different silicide patterns.

9. The MML semiconductor device of claim 1, further comprising a gate poly oxide layer interposed between the sidewall of the polycide gate electrode and the spacer.

10. The MML semiconductor device of claim 1, further comprising the gate poly oxide layer, a nitride layer, and a medium temperature oxide layer are sequentially interposed in a direction from the sidewall of the polycide gate electrode to the spacer.

11. The MML semiconductor device of claim 1, further comprising the gate poly oxide layer and the medium temperature oxide layer are sequentially interposed in a direction from the sidewall of the polycide gate electrode to the spacer.

12. The MML semiconductor device of claim 1, further comprising an interlayer dielectric overlying the polycide gate electrode and the NMOS and PMOS gate electrodes,

wherein a silicide blocking layer in which the medium temperature oxide layer and the nitride layer are sequentially stacked is interposed between the spacer and the interlayer dielectric.

13. A method of manufacturing a memory merged logic (MML) semiconductor device, the method comprising the steps of:

(a) preparing a semiconductor substrate on which a memory area and a logic area are defined, and on which an isolation layer and a gate oxide layer formed on an active region defined by the isolation layer have been formed;

(b) forming a gate conductive layer comprised of silicon on the memory area and the logic area;

(c) lowering a height of the gate conductive layer formed on the memory area and implanting a predetermined conductive type of impurities into the lowered gate conductive layer; and

(d) forming a silicide layer only on the lowered gate conductive layer on the memory area using deposition and photolithography, wherein the top surface of the silicide layer is lower than the top surface of the gate conductive layer formed on the logic area.

14. The method of claim 13, wherein step (c) further comprises the steps of:

(c1) forming a photoresist pattern on the logic area;

(c2) etching the gate conductive layer formed on the memory area by an etching process that uses the photoresist pattern as an etch mask and making the gate conductive layer on the memory area lower than the gate conductive layer on the logic area; and

(c3) performing an ion implantation process to implant a predetermined conductive type of impurities into the lowered gate conductive layer on the memory area.

15. The method of claim 13, wherein step (d) further comprises the steps of:

(d1) forming a silicide layer on the memory area and the logic area, wherein the top surface of the silicide layer formed on the memory area is lower than the top surface of the gate conductive layer formed on the logic area;

(d2) forming photoresist pattern on the silicide layer formed on the memory area;

(d3) removing the silicide layer formed on the logic area using the photoresist pattern as an etch mask; and

(d4) removing the photoresist pattern.

16. The method of claim 13, further comprising, after step (d), the steps of:

(e1) forming hard mask patterns comprised of nitride on portions in which the gate electrodes will be formed on the memory area and the logic area;

(f1) forming the polycide gate electrode doped with predetermined impurities and the NMOS and PMOS gate electrodes doped with no impurities on the memory area and the logic area, respectively;

(g1) implementing lightly doped drain (LDD) structures having a conductive type of impurities required in the memory and logic areas by an ion implantation process;

(h1) sequentially forming a nitride layer and an oxide layer over the entire surface of the semiconductor substrate in which the LDD structures have been implemented;

(i1) selectively removing the oxide layer formed only on the logic area; and

(j1) removing a nitride layer formed on the logic area and a hard mask pattern formed on the NMOS and PMOS gate electrodes by a wet etching process.

17. The method of claim 16, wherein, in step (f1), the gate oxide layer is used as an etch stop layer.

18. The method of claim 16, wherein the oxide layer formed in step (h1) is a medium temperature oxide layer.

19. The method of claim 16, further comprising, after step (j1), the steps of:

(k1) forming a spacer comprised of nitride along the sidewall of the polycide gate electrode and the NMOS and PMOS gate electrodes;

(l1) implanting a predetermined conductive type of impurities into the memory area and the logic area to form source/drain regions, while implanting a predetermined conductive type of impurities into the NMOS and PMOS gate electrodes;

(m1) exposing the top surface of the NMOS and PMOS gate electrodes and the source/drain region formed on the logic area by a wet etching process;

(n1) forming a silicide pattern, which is self aligned on the top surface of the NMOS and PMOS gate electrodes and the source/drain region on the logic area, by a self-aligned silicide (SALICIDE) process;

(o1) forming an interlayer dielectric over the entire surface of the semiconductor substrate; and

(p1) forming a self-aligned contact (SAC) electrically connected with the source/drain region formed on the memory area by a SAC process.

20. The method of claim 19, further comprising, prior to step (m1), the step of selectively forming a silicide blocking layer, in which a medium temperature oxide layer and a nitride layer are sequentially stacked, only on the memory area.

21. The method of claim 13, further comprising, after step (d), the steps of:

(e2) forming a hard mask pattern comprising a nitride and a photoresist pattern on portions in which the gate electrodes will be formed on the memory area and the logic area, respectively; and

(f2) forming a polycide gate electrode doped with predetermined impurities and NMOS and PMOS gate electrodes doped with no impurities on the memory are and logic area, respectively, by an etching process that uses the hard mask pattern and the photoresist pattern as an etch mask.

22. The method of claim 21, wherein, in step (f2), the gate oxide layer is used as an etch stop layer.

23. The method of claim 21, further comprising, after step (f2), the steps of:

(g2) removing the photoresist pattern;

(h2) implementing LDD structures having a conductive type required in the memory area and the logic area by an ion implantation process;

(i2) forming a spacer comprising nitride on the sidewall of the polycide gate electrode and the NMOS and PMOS gate electrodes;

(j2) forming source/drain regions on the memory area and the logic area by an ion implantation process;

(k2) selectively forming a silicide blocking layer, in which a medium temperature oxide layer and a nitride layer are sequentially stacked, only on the memory area;

(l2) exposing the top surface of the NMOS and PMOS gate electrodes and the source/drain regions of the NMOS and PMOS by a wet etching process, while protecting the memory area by the silicide blocking layer;

(m2) performing a SALICIDE process to form a silicide pattern on the top surface of the NMOS and PMOS gate electrodes and the source/drain regions of the NMOS and PMOS;

(n2) forming an interlayer dielectric over the entire surface of the semiconductor substrate; and

(o2) forming a SAC electrically connected with the source/drain region formed on the memory area by a SAC process.